# HUNTRON

# **Huntron Test Development Information**

This Huntron Test Development information can be used to estimate the creation time of a Huntron Test using a Huntron Tracker system with an Access Prober. Huntron Technical Support personnel use their troubleshooting expertise and experience to plan the test with the goal of having the Prober replace their hands, not their skills.

The Huntron Test examples used in this guide are for estimating purposes only. Creation and test run times will vary due to board complexity and customer needs.

Scope of work will be defined as:

- Type A Full Compliment and Net Huntron Test and baseline signatures using CAD import
- Type B Full Compliment Huntron Test and baseline signatures without CAD import
- **Type C** Primary Component Huntron Test and baseline signatures using CAD import
- Type D Primary Component Huntron Test and baseline signatures without CAD import

Information about Test Type:

- Full Compliment All components and connectors are included in the test and is part of Type A and Type B test. This type of test will have the longest development times. Net based tests use all unique accessible nets and are included with the Type A tests only. CAD data is required.
- **Primary Component Test** Primary components (such as ICs, transistors, diodes, connectors) which provide coverage to a majority of PCB nets. Primary Component tests are included with **Type C** and **Type D** tests.

Scope of Work Description	Туре А	Туре В	Туре С	Type D
Determine Test objective	~	~	~	~
Confirm Huntron Test platform	~	~	~	~
Determine Test type				
Full Compliment (All components)	~	~		
Net Test (Unique PCB nodes only)	<ul> <li>✓</li> </ul>			
Primary Component Test (Semiconductors, connectors)			~	✓
Sequence and/or Scan List Breakdown	~	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	>
Board orientation and slot selection	~	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	~
Data Entry				
CAD Data	~		~	
Manual Entry		<ul> <li>✓</li> </ul>		<ul> <li>✓</li> </ul>
Determine good Common reference(s)	~	~	~	~
Adding Graphics/Instructions	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>
Range selection	~	~	~	~
Board Holder Construction (if needed)	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>
Scanning and saving of Reference signatures	~	~	~	~
Archive a backup copy of test database	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>
Testing good and bad boards to optimize test	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	<ul> <li>✓</li> </ul>	~

4.2" (10.6cm)

2.8" (7.1cm)







**Example 2:** - All surface mount

- components
- Approx. 50 ICsApprox. 25 discrete semiconductors

**Example 1:** - All surface mount components

Approx. 15 ICsApprox. 40 discrete semiconductors

- Board size: 4.2"x 2.8"

(10.6cm x 7.1cm)

Development times:

7.1 hrs

12.9 hrs 5.1 hrs

9.7 hrs

- 2 side test

Type A

Type B Type C Type D

- Board size: 9.1"x 4.2" (23.1cm x 10.6cm)

- 2 side test

#### **Development times:**

Type A	14.1 hrs
Type B	18.5 hrs
Type C	12.4 hrs
Type D	15.9 hrs

4.2" (10.6cm)

7.7" (19.5cm)



# Example 3:

- All SMD
- Approx. 170 ICs
- Approx. 5 discrete semiconductors

## Board size:

14.1" x 7.7"

- (35.8cm x 19.5cm)
- 1 side test

#### **Development times:**

- Type A 20.1 hrs
- Type B31.5 hrs
- Type C
   10 hrs

   Type D
   25.5 hrs

16.1" (40.7cm)



## Example 4:

- All SMD
- Approx. 210 ICs
- Approx. 40 discrete semiconductors
- 3 connectors
- Board size:
- 16.1" x 14.5" (40.7cm x 36.8cm)
- (requires Access 2
- Prober)
- 2 side test

#### **Development times:**

Type A	29.0 hrs
Type B	60.2 hrs
Type C	16.8 hrs
Type D	43.5 hrs

# Huntron Test Development and Test Times

Test Development Times	<b>Example 1</b> 15 ICs, -40 discrete semiconductors	Example 2 -50 ICs, -25 discrete semiconductors	<b>Example 3</b> -170 ICs, 5 discrete semiconductors	<b>Example 4</b> -210 ICs, -40 discrete semiconductors		
Data Entry Time <sup>1</sup>						
Туре <b>А</b> <sup>2</sup>	0.6 hrs	1.2 hrs	1.6 hrs	2.0 hrs		
Туре <b>В</b>	7.5 hrs	10.1 hrs	20.0 hrs	41.0 hrs		
Туре <b>С</b> <sup>2</sup>	0.4 hrs	0.9 hrs	1.0 hrs	1.3 hrs		
Туре <b>D</b>	5.0 hrs	9.5 hrs	16.5 hrs	28.0 hrs		
Test Adjustment Time <sup>3</sup>						
Туре А	5.0 hrs	11.4 hrs	16.5 hrs	24.0 hrs		
Туре <b>В</b>	3.9 hrs	6.9 hrs	9.5 hrs	16.2 hrs		
Туре <b>С</b>	3.2 hrs	10.0 hrs	7.0 hrs	12.5 hrs		
Туре <b>D</b>	3.2 hrs	4.9 hrs	7.0 hrs	12.5 hrs		
Test Completion Time <sup>4</sup>	1.5 hrs	1.5 hrs	2.0 hrs	3.0 hrs		
Total Development Time <sup>5</sup>						
Туре А	7.1 hrs	14.1 hrs	20.1 hrs	29.0 hrs		
Туре <b>В</b>	12.9 hrs	18.5 hrs	31.5 hrs	60.2 hrs		
Туре <b>С</b>	5.1 hrs	12.4 hrs	10.0 hrs	16.8 hrs		
Туре <b>D</b>	9.7 hrs	15.9 hrs	25.5 hrs	43.5 hrs		
Optional Additions <sup>6</sup>	1.0 hrs	1.0 hrs	2.0 hrs	2.5 hrs		
<b>Type A test:</b> Full Compliment and Net CTR using CAD data <b>Type B test:</b> Full Compliment CTR without CAD data						

Type C test: Primary Component CTR using CAD data

**Type D test:** Primary Component CTR without CAD data

#### Notes:

- 1 Times are based on entry by a user with strong skills in Microsoft Windows and Huntron Workstation software.
- 2 Huntron Tests created using CAD data require full ASCII layout files generated from the original CAD PCB layout software (example: Mentor Graphics neutral file file extension is .NEU). Huntron CAD Tools software (includes Unisoft ProntoView Markup software) is required for CAD import into Huntron Workstation. CAD Tools are optional and not included with Huntron Workstation.
- 3 Test Adjustment Time includes running the test routines, adjusting test range settings and setting signature references using a known good board(s).
- 4 Test Completion includes backing up of test routine, and adding complete board test instructions.
- 5 Times do not include construction of custom board holders or Optional Additions.
- 6 Optional Additions include setting up software buttons to display scanned board images, schematics, and layouts. Construction time for custom board holders is not included.